CONSIDERATIONS FOR DESIGN, INTEGRATION AND EVALUATION OF COCHLEAR IMPLANT ASIC BY ULTRA-LOW POWER TECHNIQUES

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ABSTRACT

Ultra low power techniques are most required for latest biomedical applications. Efficiency of these systems depends on the requirement of less power for their operation. To achieve this most of the bio-inspired systems have been implemented in nano technological environment. Cochlear implant is one of the most required bio-inspired systems. Various strategies for cochlear implant design have been presented in the literature. Researchers of all around the world have many positive measures of cochlear implant that can be used for the communication improvement through cochlear implant. In context of the Indian people hearing aid implantation is not cost effective. Research can be done to make cochlear implant cost effective in context of Indian people. This survey focuses on the various analysis and remedies for low power consumption. This paper goes through the national and International status in context of cochlear implant design. Also working of actual human auditory system is compared with the working procedure of cochlear implant. Working of audio components with cochlear implant has also discussed. Also this paper discusses the suggested plan of action for utilization of this study and environmental impact assessment and risk analysis on cochlear implant design.

Keywords—Bio-inspired systems, CMOS, Cochlear Implant, Leakage Power, Ultra-low power, VLSI.

I. ORIGIN OF THE STUDY

Ultra-low power CMOS digital integrated circuits are the enabling technology for the modern bio-inspired systems. The efficiency of these systems has been realized with requirement of low power for their operation. As for the fulfilment of the requirement of present technological world, we are on the way to commercialize these devices to the nano scale. Higher functionally and higher performance of biomedical circuits are required at lower power consumption. So with the growing demand of ultra-low power digital circuits for biomedical applications, study of low power VLSI design has become one of the most important factors in continuous development of these devices. This research will focuses on the various considerations in ultra low power CMOS VLSI designs for broad class of bio-inspired system architectures such as sources of power dissipation and remedies to reduce these power dissipations. Consideration of these remedies benefits in low power consumption by digital devices even below 45nm technologies. The
power dissipation has become one of the show stoppers in efficient development of microelectronics technology for biomedical systems, main reason being increase in power per unit per area due to the reduced feature size and integration of more functions per chip [1]. The scaling down of the channel length of transistor to below 0.5 μm and increase of the density of gates on chip to very high range have increased the power density more than expected. Technologies above 65nm represent a real challenge in voltage and frequency scaling. In designing of low-power, low-voltage digital biomedical circuits, portability and reliability have also played a major role. In present technological environment, reduction in the power dissipation without affecting the performance of the circuit has become necessary for biomedical systems [23].

Digital circuits in any bio inspired system, when do its functionality it consumes some power, which get dissipated in the form of heat. Digital circuits used in these devices are operated by using batteries which needs recharging or replacement. Applications powered by battery such as hearing aid, implantable pacemaker and portable electronic devices are the example of low power electronics. In some applications such as biomedical implantable devices recharging of battery is not possible frequently and also heat dissipated by these devices can be harmful for the body. Therefore, in order to reduce the heat dissipation and increase the battery life, there is a need of ultra low power designing technology which can reduce the power dissipation through the VLSI logic circuits. However, in spite of importance of low power methods in advancement of ultra low power digital VLSI design for recent technology, these power reduction methods and their comparisons have never been surveyed so far. So, there exists a gap in selection of best ultra low power techniques for designing of digital electronics which can be further used in biomedical implants. One of the essential aim of this research is to fill the existing gap by doing investigation of various ultra low power techniques and selection of best form them for implantable digital electronics. Cochlear implant is a most important device for deaf human beings and it is a mode of partial hearing for more than 120,000 persons worldwide. Cochlear System integration and evaluation will be done with respect to reliability, safety and challenges by the present technological world [4]. A cochlear implant is one of the greatest requirements of today’s medical industry. In starting phase of cochlear implant, this device is only used to provide little sensation of sound. In the 1980s, this device was available with multiple channels of data processing and multiple sites of stimulation but at that time these systems were with higher levels of speech reception than their single-channel. After late 1980s to present technological world, various improvements have been done in this device with the use of new and better processing strategies and multi-electrode implants world [5]. So, this study will also focus on design, integration and evaluation of biomedical cochlear ASIC design by implementation of best selected low power technology.
II. REVIEW OF STATUS OF RESEARCH AND DEVELOPMENT IN THE SUBJECT

A. Techniques for ultra-low power design

Power and area consumption are one of the basic parameters which acts as a key limitation in many electronic biomedical systems. Power and area consumed by the various biomedical applications should be less as possible. So there is requirement of some new power and area efficient VLSI designing techniques and methodologies which can limit power and area consumption. Due to cascading operations, circuits are becoming more efficient but may use more transistors to implement complicated functions. This leads to more power consumption. Some biomedical applications require the circuit to be implanted inside the body. This requires the circuit to be implemented with small area and power harvesting techniques. So the design of power efficient VLSI design methodology has become most important and essential for the researchers. Total power dissipation in any CMOS circuit is sum of static, dynamic and short circuit power dissipation [6-7].

B. International status in context of Ultra Low Power Designs

1. Static power reduction techniques

Static power consumption is directly proportional to the summation of leakage current in the circuit hence static power consumption can be reduced by reducing static current consumed by the circuit. Some circuit designing techniques consumes large power, so circuit designed by these techniques can be turned off when operations from these circuits are not needed. This can result in reduction of the static power consumption. Leakage current can be limited by threshold voltage increase and substrate voltage increase, reducing the gate source voltage, drain source voltage and temperature. Static power consumption acts as a limiting factor for battery powered design and it increases exponentially with the decrease of power supply and threshold voltage [6]. Another method to control leakage current is application of reverse body bias and use of low threshold voltage device during idle mode. Opposite can be used in active mode i.e. application of forward body bias and use of high threshold voltage device. Another method to reduce static power consumption is turning off the supply voltage completely. This can be achieved by using voltage regulator externally and using series transistor internally [8]. Also multiple threshold circuits can be used in which low threshold transistors are used for actual logic implementation and high threshold transistors can be used as to disconnect the power supply during active mode. High threshold voltage is connected between true voltage $V_{DD}$ and virtual voltage $V_{DDV}$. The extra high threshold transistor increases the impedance between true and virtual power supply. By pass capacitor has been used to stabilize the supply voltage. MTCMOS is suitable for low voltage device by using very wide high threshold voltage transistor.

2. Various static power reduction techniques

Various static power reduction techniques have been presented in the literature. In [9-10] a dual threshold technique has been used to reduce power. High threshold transistors are used in the leakage
path and for gating the supply voltage so as to reduce leakage in unused part of the circuit where as in [11] a current limiter has been used to reduce switching noise and the static power dissipation instead a current source. In [12] input vector control method is used for leakage power minimization in static CMOS circuits and Boolean functions have been used to model leakage effects whereas in [13] reduced V<sub>DD</sub> supply is used for the reduction of static power consumption. Although in CMOS circuits the threshold voltage reduction is beneficial in terms of speed but it shows its disadvantage in terms of increased sub threshold leakage current which is one of the main reasons of static power dissipation. In [14] a new technique called LECTOR (LEakage Control TransistOR) has been introduced for designing digital circuits which can reduce leakage current without increasing other sources of power dissipation. In LECTOR technique NMOS and PMOS transistors are used as a leakage control transistors. Out of two extra connected transistors one will be always near to its cut-off.

In [15] a new methodology for ASIC design has been introduced which shows a lot of advantage in VLSI design as compared to MTCMOS. Proposed design methodology is based on the use of modified standard cells which help in reduction of leakage currents when cell remains in standby mode and also allow precise estimation of leakage current. Minimization of the leakage in the pull-down network has been done when input to the standby cell results in high output, and similarly minimization of leakage in the pull-up network takes place when output has a low value. In this manner, two low-leakage variants of each standard cell are obtained. New methodology has shown its efficiency in terms of speed and area as compared to MTCMOS designing technique. This methodology avoids the unpredictability of leakage MTCMOS design. Introduced inverting H/L cells utilize exactly one supply gating devices compared to MTCMOS designing technique. These cells also provide less delay characteristics as compared to the MTCMOS. According to the report of International technology roadmap for semiconductors (ITRS) [16] total power consumption may be dominated by static power dissipation when there will exist technology scaling. Leakage power can be considered negligible till 0.18μm technology and above but when the technology decreases below 0.18μm static powers can become the top most concern while VLSI circuit design.

In [17] common V<sub>DD</sub> and V<sub>SS</sub> technique has been used to overcome the semiconductor leakage. As the technology scaling comes in to existence, static power dominates the total power consumption [18]. Sub-threshold leakage is main source of static power consumption and this leakage arises by creating a weak inversion channel between drain to source [19]. Another factor that is responsible for leakage is gate oxide leakage which comes in to existence due to tunneling current through gate oxide i.e. channel punch through current and gate current due to hot-carrier injection. Thickness of gate-oxide gets reduced due to technology scaling. Although this is beneficial in terms of area but causes sub-threshold leakage.

A survey of techniques for minimization of leakage power has been presented in [20]. These techniques range from cell-level to architectural level solutions that will help in efficient system-level design. However in [21] stacked sleep transistor has been used to make the circuit power efficient. Subthreshold leakage can be reduced taking the advantage of stack effect i.e. by using stacking transistor. The stack
effect comes into existence when two or more stacked transistors are turned off together which is one of the main reasons for reduced leakage power consumption. Also various other reasons of power dissipation and power efficient approaches have been presented by the authors. Parametric analysis of various leakage reduction techniques provides a suitable choice for selection of leakage power minimization technique for low power VLSI applications. In [22] an overview of all above explained low leakage technologies has been presented. Some new techniques can be implemented to reduce leakage power consumption. Some of new effective method introduced in [23] are dynamic voltage and frequency scaling (DVFS), dynamic power switching (DPS), adaptive voltage scaling (AVS) and static leakage management (SLM).

3. DYNAMIC POWER REDUCTION TECHNIQUES

Dynamic power dissipation becomes dominant when design technology with high threshold voltage and oxide thicknesses is chosen for chip design. By decreasing some factors such as switching capacitance, supply voltage, operating frequency and activity factor dynamic power consumption can be reduced [24]. Dynamic circuit families have very high activity factor hence consume very high dynamic power. Clock gating is one of the techniques which can be used to stop that part of circuit which remains ideal for a long time. In [25] some methods of low power design are described by the authors to reduce dynamic power dissipation. These are clock gating, gate level power optimization, multiple V\textsubscript{DD} technique and multiple threshold devices. As dynamic power dissipation is proportional to square of V\textsubscript{DD}, so by introducing different V\textsubscript{DD} for different blocks can help in reduction of total power consumption at the price of increased delay. Comparison of these different techniques is described in Table 3.

Dynamic power management techniques can be used to lower dynamic power consumed in various level of abstraction and it is defined as a design methodology with a minimum number active components or a minimum load on such components. Dynamic power management consists of a set of techniques that achieves power efficiency by reducing the performance of system components when they remain in ideal state [26] whereas Dynamic power management has been explained as technique of extending battery life by using same technique in [27]. Advantage and disadvantage of various leakage reduction techniques has been shown in Table 1. A conclusion of various power reduction techniques have been shown in Table 2 and comparisons of dynamic power reduction techniques such as multiple threshold, clock gating and multi voltage in terms of power benefit, timing penalty, area penalty, impact on architecture, impact on design, impact on verification and impact on place & route have been shown in Table 3.
III. INTERNATIONAL STATUS IN CONTEXT OF COCHLEAR IMPLANT DESIGN

Various strategies for Cochlear Implant Design have been presented in the literature. Researchers made aware about wide range of sound processing schemes for cochlear implants designs named as Programmable Interactive System for Cochlear Implant Electrode Stimulation (PISCES) and it was designed and tested at Lincoln Laboratory and then installed at the Cochlear Implant Research Laboratory (CIRL) of the Massachusetts Eye and Ear Infirmary (MEEI) [28]. Difficulties have been faced by hearing-flawed people, and particularly hearing-assistance and cochlear-implant users, if they want to communicate over the telephone. The clarity of telephone voice is less than the clarity of face-to-face voice. A Bluetooth powered wireless phone adapter has been introduced by the researchers that can be used for routing the signal to the cochlear implant processor [29]. A 3-D reconstruction method of cochlear implant electrodes is proposed in [30] to localize individual electrodes from two X-ray views in combination with the spiral computed tomography technique. A novel speech processing strategy that encodes both amplitude and frequency modulations in order to improve cochlear implant performance in noise has been proposed in [31].

A cochlear implant processor has been introduced in [32] on a 1.5- m BiCMOS technology which consumes 211 W power and 77-dB dynamic range of operation. The 9.58 mm 9.23 mm processor chip runs on a 2.8 V supply and has very less power consumption. This processor can be used in fully implantable hearing aid. An approach that can be used for cochlear implant DSP is proposed in [33] which have ability to solve the data rate problem.

A power management unit (PMU) for an autonomous wireless sensor of cochlear implant has been presented in [34]. A mixed-signal VLSI chip that challenge nonlinear active cochlear signal processing has been presented in [35]. 2.45-GHz complementary metal–oxide–semiconductor (CMOS) ultra-low-power transmitter suitable for cochlear implant application has been introduced by the researchers that are energy self-efficient and have small area [36]. The speech production and natural language model of cochlear implant users with respect to environmental changes has been analysed by the researchers. A mobile personal audio recording from continuous single-session audio streams has been used in [37].
Table.1 Advantages and disadvantages of Leakage Reduction Technique

<table>
<thead>
<tr>
<th>Technique</th>
<th>Advantages</th>
<th>Disadvantage</th>
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<tbody>
<tr>
<td>Forced stacking</td>
<td>Easy to implement, Leakage savings, Easy to fabricate</td>
<td>Propagation delay increases.</td>
</tr>
<tr>
<td>Sleepy Stack</td>
<td>Single threshold transistors, Less delay compared to force stacking approach.</td>
<td>Sleep transistors need control circuit, Area increases, Less power savings</td>
</tr>
<tr>
<td>Input Vector Control</td>
<td>High power savings compared to Forced stacking technique.</td>
<td>Control circuit is very complex, Exhaustive simulations required</td>
</tr>
<tr>
<td>Power gating with stacking</td>
<td>More leakage savings in both operating modes</td>
<td>Delay increases, Area increases, Complex to fabricate</td>
</tr>
<tr>
<td>Power gating with PMOS and NMOS sleep transistor</td>
<td>Large power savings, most preferred method</td>
<td>Control circuit is needed</td>
</tr>
<tr>
<td>SCCMOS with PMOS and NMOS sleep transistor</td>
<td>Best power savings, Easy to fabricate</td>
<td>Control circuit is needed</td>
</tr>
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Table.2 Power reduction Methods

<table>
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<tr>
<td>• Static Leakage Management</td>
<td>• Multiple Vdd</td>
<td>• Adiabatic Circuits</td>
</tr>
<tr>
<td>• By Increasing the threshold voltage and substrate voltage</td>
<td>• Multiple Threshold Voltage</td>
<td>• Variable Body Biasing</td>
</tr>
<tr>
<td>• By reducing the gate source voltage, drain source voltage and temperature</td>
<td>• Clock Gating</td>
<td>• Dynamic Threshold MOS</td>
</tr>
<tr>
<td>• By using multiple threshold circuits</td>
<td>• Gate level Power Optimization</td>
<td>• Logic Design For Low Power</td>
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<tr>
<td>• Computation-based guarding technique</td>
<td></td>
<td>• Reducing Glitches</td>
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<tr>
<td>• LECTOR technique</td>
<td></td>
<td>• Logic Level Power Optimization</td>
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<tr>
<td>• Adaptive voltage scaling</td>
<td></td>
<td>• Standby mode leakage suppression</td>
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<td></td>
<td></td>
<td>• Dynamic Power Suppression</td>
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Ultra-low power VLSI designs can be attained at various design consideration layers i.e. on system level, algorithm level, architecture level, circuit level and technology level. Power efficient design can be achieved by exploring different low power alternatives at different layer of abstraction as well as by using proper power estimation tool that can provide accurate feedback on quality of low power design [41].

Optimization at different abstractions level can be achieved by following low power design methodology [42] and dynamic / hybrid guarding. As each time when a sleep transistor is activated it consumes some dynamic power. A lid on important performance parameters of circuit efficiency has been put in [45].

Optimization of one parameter may be achieved by the inefficiency in another parameters. Introduced

### IV. NATIONAL STATUS

#### A. National status in context of Ultra Low Power Designs

Ultra-low power VLSI designs can be attained at various design consideration layers i.e. on system level, algorithm level, architecture level, circuit level and technology level. Power efficient design can be achieved by exploring different low power alternatives at different layer of abstraction as well as by using proper power estimation tool that can provide accurate feedback on quality of low power design [41].

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Optimization of one parameter may be achieved by the inefficiency in another parameters. Introduced

<table>
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<tr>
<th>Technique</th>
<th>Power Benefit</th>
<th>Timing Penalty</th>
<th>Area Penalty</th>
<th>Impact on Architecture</th>
<th>Impact on Design</th>
<th>Impact on Verification</th>
<th>Impact on Place &amp; Route</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiple threshold</td>
<td>Medium</td>
<td>Little</td>
<td>Little</td>
<td>Low</td>
<td>Low</td>
<td>None</td>
<td>Low</td>
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<tr>
<td>Clock gating</td>
<td>Medium</td>
<td>Little</td>
<td>Little</td>
<td>Low</td>
<td>Low</td>
<td>None</td>
<td>Low</td>
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<tr>
<td>Multi Voltage</td>
<td>Large</td>
<td>Some</td>
<td>Little</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
<td>Medium</td>
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LECTOR technique is found to be more effective in both ON and OFF mode of operation and is applicable for high speed circuits.

B. National status in context of Cochlear Implant Design

A top story by Murali Krishnan on 14.11.2014 introduced about low cost home-grown Cochlear Implants which had been invented by Indian researchers. Researchers said that they are close to clinical trials for a low-cost cochlear implant, which could help thousands of people in India. The Defence Research and Development Organization (DRDO), had completed two year-long and planned to launch indigenously-designed implant for commercial production in end of 2014 [46].

As per times of India on Oct 15, 2015, DRDO set to realise a device for deaf kids. Three laboratories of the Defence Research Development Organization (DRDO) at the point to realising their dreams of produce the world's cheapest cochlear implant. This proposed implant is also approved for human clinical trials from next year at eight different institutions in the country including Post Graduate Institute of Medical Education and Research (PGIMER), Chandigarh. Imported implants cost between Rs 6 lakh and Rs 7 lakh and the indigenous ones will be cheaper by one-fourth of this. Also the DRDO device has been approved by the Drugs Controller General of India for clinical trials [47].

Fig.2. News article of Clinical trials of cochlear implant article in The Hindu [48]

In [43-44] a pre-computation-based guarding technique has been presented to decrease power consumptions in CMOS VLSI circuits. Sleep transistor with increased threshold has been placed in series with the some part of the CMOS VLSI circuit. Input values to the designed circuit are used to turn on and off this sleep transistor which results in decrease of static as well as dynamic power. Two modifications to the pre-computation-based guarding technique have been introduced to improve the power saving. These techniques are reduction in the switching activity of sleep transistors.
V. IMPORTANCE OF THE STUDY IN THE CONTEXT OF CURRENT STATUS

Hence, Ultra low power biomedical digital electronics has gained significant attention in healthcare industry, where digital biomedical devices are becoming widespread for use in the diagnosis of disease or other conditions, or in the cure, mitigation and prevention of disease. They are used in wide variety of conditions such as cardiac pacemakers for cardiac arrhythmia, cochlear implants for deafness or retinal implants for blindness. A large amount of activity is being researched in brain-machine interfaces for paralysis, stroke, and blindness. Biomedical devices based on ultra low power techniques are one of the key requirements for most of biomedical electronic systems. In recent trends of the medical industry ultra low power techniques can give their efficiency in implantable and wearable devices. In other words, ultra low power digital biomedical devices act as an interface between biological and digital world. Several test chips have proven the possibility of designing high performance ultra low-power low-voltage converters in nanometre CMOS technologies. According to performance requirements a proper ultra low power technique should be carefully chosen so that performance of digital design met with the requirement of minimum power consumption. For applications such as portable devices or implanted biomedical devices where power is extremely limited, it is of great interest to investigate the tradeoffs between performance and power consumption. The biomedical devices often operate only with a battery, e.g., blood glucose monitor, pacemaker. Therefore, it is desirable to fully utilize the energy without sacrificing the performance of the system. To achieve the ultra low power consumption, various techniques should be explored from system level to circuit level.

The cochlear implant is one of the most favourable auditory unreal designs developed till date. It is the most compelling unreal design in terms of re-habitation of function. An analysis of recent cochlear implants has been presented in [49]. However an impressive progress has been made in the advancement of cochlear implants but there are so many field still remained for improvements, especially low power and area design of cochlear implant. Being a most successful neural artificial design, cochlear implants have provided partial hearing to more than 120 000 persons worldwide. Biomedical engineers have played a main significant role in the design, integration and evaluation of the cochlear implant system, but the overall success will be achieved when cochlear implants will be available with less cost and good efficiency in terms of less power consumption.

However, in spite of importance of low power methods in advancement of ultra low power digital VLSI design and digital biomedical electronics for recent technology, these power reduction methods, low power technologies and their comparisons have never been surveyed so far. So, there exists a gap in selection of best ultra low power techniques for designing of digital electronics which can be further used in biomedical implants.
Following are the main points of research justification:

- This research will provide a comparative study of various ultra low power technologies to various research communities.
- By following this research, designing industry will be able to select a best possible digital design for biomedical digital devices.
- Use of energy harvesting techniques can provide future advance in the area of implantable medical devices [50]. This research will also provide a comparative analysis of various energy harvesting and adiabatic techniques that can provide a forward looking projection in the field of implantable medical devices.
- Research in Digital biomedical electronics in India has become a dominant science in 21st century because of its big impact on society. However this will happen if it will interacts successfully with three key areas [51] shown in Fig.3.
- As there will be the demand of power efficient cochlear design, this research will focus on Design, Integration and Evaluation of Cochlear Implant ASIC by Implementation of best selected ultra low power technique.

Society is the one in which the research is dropped and for whom it can solve the grand challenges. Country act as its nurturing ground of scientific excellence and the world is one which will offer competition and collaboration. This project will successfully interact with these three key areas.
A. How hearing works

1. Audio signal enter the ear and transit along the ear canal to the ear drum.
2. Vibrations take place in the bones of middle part of ear due to the movement of the signal in the eardrum.
3. These vibrations are spread up to cochlea which is an inner part of the ear filled with fluid.
4. Tiny hairs covering this inner ear pick up these movements and send them as an electrical signal to the brain. Brain takes these signals and understands it as a sound.

**Fig.4. Steps involved in human hearing [52]**

B. Hearing with a cochlear implant

1. Audio processor pick up audio with the help of microphones and the audio processor converts the audio into digital form of information.
2. This digital information is passed through the coil to the implant.
3. The implant transfers the electrical form of the signals to the electrode of the cochlea implant.
4. The hearing nerve fibres in the cochlea catch up the signals and transfer it to the brain, so as to give the giving the impression of sound.

**Fig.5. Steps involved in hearing with cochlear implant [52]**
C. How the audio components works

1. Hearing aids, which acts as an audio components amplifies these obtained audio signals and transfers these signal via the normal hearing pathway.
2. Processor used in these hearing aids converts audio signals in to digital signal which is further sent to the implant under the skin.
3. The implant moves electrical signals to the electrode into the cochlea, exciting the nerve fibres.
4. These nerve reactions are sent to the brain, where these reactions are combined with amplified sounds from the audio component into a recognised sound.

![Fig.6. Steps involved in working of audio components [52]](image)

So, by taking care of requirement of low power and area consumption along with working style of human hearing the proposed methodology for the digital cochlear implant design has been divided into four main phases:

a. Survey of existing ultra low power technique
b. Design and analysis of circuits of cochlear implant by using existing technologies
c. Computer simulations for the designed circuit in terms of power consumption
d. Design and optimization of cochlear implant ASIC designed by best selected ultra low power technologies

VI. SUGGESTED PLAN OF ACTION FOR UTILIZATION OF STUDY OUTCOMES

The impact deafness can varies depending upon the age. Adults as well as children can acquire deafness experience while communication, this may results in occupational option reduction and increase the feelings of public detachment. The impact on deafened in children by birth is much greater. Many deafened children establish marked language and delays in their education. Although a number of researchers have checked the social and physical effectiveness after cochlear implantation in world wide. The influence of cochlear implantation should be measure not only by its practical efficiency but how it is changing the quality of life of deaf people. Majority of population who made the used of cochlear implant are those who
acquire deafness after the acquisition of language i.e. post-lingual deafened. These adults are having very less audio input, so they had difficulty in getting speech of other but this is not affecting their audio production skills. With the help of cochlear implant, post-lingual deafened adults are capable of having audio signals same as that of the normal audio input. The task of the implant is to fill the gap between degraded audio and good representation of audio.

Refinement in the internal structure of the cochlear implant is continuously taking place from last 20 years and this yielded increase no of audio word recognition in deaf population. The main benefits of the cochlear implant are speech perception and word recognition. However implantation of cochlear in children with pre-lingual deafness is making its impact on all aspects of their communication and this is making effect on their communication abilities [53].

Researchers of all around the world have many positive measures of cochlear implant that can be used for the communication improvement through cochlear implant. In context of the Indian people hearing aid implantation is not cost effective. Research can be done to make cochlear implant cost effective in context of Indian people [54].

VII. ENVIRONMENTAL IMPACT ASSESSMENT AND RISK ANALYSIS

As per the WHO report of 2003 survey 63 million people suffering from significant auditory loss in India. The current onset deafness in adults of India was found to be 7.6% and in childhood was 2%. Earlier during 1977–80, a multicentre collaborative study on the prevalence and aetiology of hearing impairment was done by the Indian Council of Medical Research (ICMR) at 4 centres: Calcutta (Kolkata), Delhi, Madras (Chennai) and Trivandrum (Thiruvananthapuram) on a total of 11 665 persons in rural areas and 10 935 in urban areas. As per this study fact of being impaired was found to be 10.2%. People with critical hearing loss were investigated for 24.4% and with less hearing loss was 5.9%. Hearing loss in rural areas was much greater as compared to urban areas. The National Sample Survey (NSS) 58th round (2002) surveyed disability both in urban and rural households and found that hearing disability was the second most common cause of disability after locomotors disability. Hearing loss accounted for 9% of all disabilities in the urban and 10% in the rural areas. Depending upon the extent of a person’s inability to hear properly, the degree of hearing disability was ascertained. It was estimated that the number of persons with hearing disability per 100 000 persons was 291; it was higher in rural (310) compared with urban regions (236). In the same survey, about 32% of people had profound (person could not hear at all or could hear only loud sounds) and 39% had severe hearing disability (person could hear only shouted words). The survey results revealed that about 7% of people were born with a hearing disability. About 56% and 62% reported the onset of hearing disability at >60 years of age in the rural and urban areas, respectively. The incidence of hearing disability in the past 1 year was reported to be 7 per 100 000 population. The magnitude of milder degrees of hearing loss and unilateral hearing loss would be larger than these estimates for bilateral hearing loss. The major causes of hearing loss and ear disease in India have been listed by the WHO survey. Ear wax (15.9%) was the most
common cause of reversible hearing loss. A non-infectious cause such as ageing is the next most common causes of auditory impairment in India (10.3%). Middle ear infections such as chronic supportive otitis media (5.2%) and serous otitis media (3%) are other leading causes of hearing loss. The other causes include dry perforation of tympanic membrane (0.5%) and bilateral genetic and congenital deafness (0.2%). The NSS 58th round also enquired about probable causes [55-56].

From above survey it can be concludes that in India hearing loss varies with the environment which can affect the efficiency of the developed model. This research will be based on the assessment of outcome of cochlear ASIC design taking in account Area and Power as main factors. Other factors like environment change in India, noise pollution in the particular area of INDIA can affect the performance of the proposed system. So, these factors can be the factor of risk during and after the project development.

CONCLUSION

In current medical industry there are requirement of ultra low power bio-inspired systems. From the literature survey it can be concluded that: A lot of work on power reduction techniques has been presented in the literature, but there exists a gap that performance efficiency of power reduction techniques cannot be achieved in terms of all parameters simultaneously. Although, bio-medical devices can be designed by lesser transistor count but output waveform efficiency can’t be achieved in these devices. So, there exists a gap in carefully choosing the best ultra low power VLSI design technique for implantable electronics. Cochlear implant is one of bio-inspired system which should be designed with technical and physical efficiency. Researchers have explored many measures of cochlear implant that can be used for design improvement. In context of the Indian people hearing aid implantation is not cost effective. Research can be done to make cochlear implant cost effective in context of Indian people.

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