VLSI DESIGN OF POWER EFFICIENT 4-BIT SIGNED ADDER FOR ARITHMETIC APPLICATIONS

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ABSTRACT

Area efficient ultra low power CMOS digital integrated circuits are one of the emerging technologies for the modern portable systems. Requirement of fewer transistors on chip and less power consumption for the operation of these devices proves the efficiency of these systems. To achieve the efficiency of these devices in terms of area and power, we are on the way to design these devices by using nano technologies. Higher functionally and higher performance of digital circuits at lower power consumption can also be achieved if the required output can be obtained by adding few more transistors in already used circuits in that device. An area-power efficient 42T 4-Bit Signed Adder design presented can be tested for functionality using an already designed full adder module. PTL technique based signed adder has been designed on 120nm technology using 21 each of NMOS and PMOS transistors. Three PTL 10-T full adders and one half adder modules has been used in cascade operation to achieve the output of this 4-Bit Signed Adder. Area and power efficiency is achieved in the proposed PTL design as compared to CMOS, TG and GDI technologies. DSCH 3.1 and Microwind 3.1 designing tool was used to design and simulate the proposed adder circuit on 120nm technologies. Variation in power dissipation with respect to the $V_{DD}$ has been analyzed using BSIM-4 and LEVEL-3 empirical models. The simulation results on 120 nm technology show that the proposed design consumes an area of 630.4 µm2 and a power of 7.877µW at $V_{DD}$ of 1.2V using LEVEL-3 model.

Keywords-BSIM-4, Gate Diffusion Input, Low area design, NMOS, PMOS.PTL, Transmission Gate, Signed adder.

INTRODUCTION

Any digital circuit with power on whether performing its function or not, consumes power, which is dissipated as heat. Based on the process of power dissipation there are three major sources of power dissipation in CMOS circuits [1]:

1. **Static dissipation** occurs due to the leakage current, subthreshold conduction, junction leakage and tunneling through gate oxides.
2. **Dynamic dissipation** caused by switching of transient current, and charging/ discharging of load capacitances.
3. Short circuit dissipation is attributed to short circuit current that arises when pair of NMOS and PMOS transistors conduct simultaneously.

In present day technology scenario due to the increased use of portable electronic devices, power and area efficiency has become a major concern for circuit designers. As direct implementation of area and power efficient technologies on designing platform cannot be cost effective so before actual implementation of these digital circuits on layout it is necessary to take estimation criteria in to consideration on transistor level designing [2]-[3]. So, there is a need of ultra low power designing technology which can reduce the power dissipation as well as area of the VLSI logic circuits. Digital circuits with area and power inefficiency have become one of the show stoppers in efficient development of nanoelectronics digital circuits and main reason for this is reduced factor of lambda and increased number of functions on a same chip [4]. Decrease in feature size of transistor to a large extent and increase of the number of gates on chip to very high range have increased the power density on portable devices more than expected[5-6]. Average power over the interval of time in any digital circuit is given by [1]

$$P_{av} = \frac{E}{T} = \frac{1}{T} \int_{0}^{T} i_{DD}(t)V_{DD}dt$$ (1)

In arithmetic processing unit of some portable devices, there is requirement of area and power efficient signed and unsigned adder design. The critical path in VLSI circuit design is delay provided by the MOSFETs used for the designing of these devices [7]. There is a need of more efficient signed adder design for VLSI applications. Like any other digital circuit two most important parameters of efficient signed adder design are power consumption and propagation delay, which generally work against each other. If one tries to reduce the delay the power consumption increases and vice-versa, hence, most of the architectures choose one of the two important design parameters as per their application requirements.

Different designers come up with different architecture and different implementation by exploiting different circuit design techniques [8]. Traditional CMOS technology is used to achieve accurate output with full voltage swing at the cost of large area attributed to use of complementary transistors, whereas Transmission Gate (TG) technology consumes less area as compare to CMOS technology. Another logic that consumes less power and area as compared to CMOS and TG technology based design is pass-transistor logic (PTL). High speed, less power dissipation and less interconnection effects are some of the main advantages of PTL technology [9]. The advantages of the PTL come at a cost, the threshold drop across the single-channel pass transistors and the static power dissipation. These problems can be overcome by Complementary Pass-transistor Logic (CPL) as it features complementary inputs/outputs based on NPTL logic. In arithmetic and computing applications, 4-Bit Signed Adder is the circuit which can give signed addition of two signed 4 bit numbers. Addition being the fundamental arithmetic operation an adder circuit can be used to implement not only addition but, subtraction and multiplication as well. If we can improve the performance of the adder module we are actually improving the performance of the whole arithmetic unit in any computing device. This efficiency
improvement in the most sought after in the portable battery operated electronic devices. Block diagram description of a 4-Bit Signed Adder using the full adder as a module is shown in Fig.1.

Fig.1. A generic 4-Bit Signed Adder using a Full Adder as building block

**VLSI DESIGNS OF FULL ADDER MODULES**

Adder is one of the basic digital circuits used in various portable electronics. There are different designing technologies that can be used to design this basic module to save power and area. To analyze performance of any digital circuit there are some of main parameter estimation criteria - Area Consumption, Speed and Power Consumption. These criteria’s should be investigated and analyzed as per the application and logic styles [10]. A schematic of CMOS full adder design has been shown in Fig 2, which has been designed by equal number of PMOS and NMOS devices. Due to complementary use of MOS transistors full voltage swing can be obtained at the output waveform. This adder design is made by 36 transistors. Sum output has been obtained by using cascade operation of half adder and a 2x1 6T MUX has been used to obtained carry output. Operation of CMOS full adder has been shown for \(ABC = 111\), glowing output LED is showing high output.
Fig. 2. CMOS Full Adder Design [10]

Also operation of transistor as an open and close switch is also shown for same input. TG Full adder design by using 22 MOS transistors has been shown in Fig 3 [10]. Although adder designed by CMOS and TG technologies give full voltage swing at the output which is best for cascade operation, but it consume high power and area.

Fig. 3. CMOS Full Adder Design [10]

In [10] it has been proved that if one designing style is good in terms of one of estimation parameter it can give degraded performance in terms of another parameter. The major share of the total power dissipation in CMOS VLSI circuits is of dynamic power dissipation. This is the power dissipated due to charging and discharging of capacitor driven by any digital circuit. If a load C is switched between ground and supply voltage than load will charge and discharge according to switching frequency. Current flows from $V_{DD}$ to the load to charge the load capacitance and from the load to ground to discharge the same. Average dynamic power dissipation in any CMOS VLSI circuit is given by

$$P_d = \frac{1}{T} \int_0^T i_{dd}(t)V_{dd}dt = \frac{V_{dd}}{T} \int_0^T i_{dd}(t)dt$$  \hspace{1cm} (2)
\[ \frac{V_{DD}}{f} [T_{sw}C_{VDD}] = C_{VDD}^2f_{sw} \]  

(3)

But in any practical application there are only few gates that switch at every input clock. So switching frequency in equation (3) can be rewritten as multiplication of activity factor and clock frequency. Now dynamic power dissipation can be given by equation (4):

\[ P_D = \alpha C_{VDD}^2f \]  

(4)

Where \( \alpha \) is the activity factor, \( C \) is the load capacitance, \( V_{DD} \) is the supply voltage and \( f \) represents operating clock frequency. Disadvantage of full CMOS and TG technologies can be overcome by exploiting the PTL designing technology wherever the target application constraints can be met. A full adder design by using Pass Transistor Logic has been shown in Fig 4, implemented by using 10 transistors only. This design consumes less area as compared to Full CMOS and TG full adder designs. Although PTL adder design consumes less area as compared to CMOS and TG design but it shows its inefficiency in terms of degraded output swing. Due to this disadvantage circuit designed by this designing technique are not suitable for and cannot be used in cascade operation.

![Fig 4. PTL Full Adder Design [10]](image)

A new and area efficient full adder design has been implemented in [10] Fig 5 by using a new designing technique called GDI. Adder circuit implemented by using this technique shows it area and power efficiency as compared to CMOS, TG and PTL technologies. This efficiency has been achieved by simultaneously generation of XOR and XNOR output, that acts as input for the SUM and CARRY Module of full adder. Sum and Carry output has been obtained by using 2x1 MUX designed by using only two complementary transistors.
4-BIT SIGNED ADDER SCHEMATICS

Proposed 4-Bit signed adder design has been implemented by cascade operation of three full adder modules and one half adder module shown in Fig. 6. Hexadecimal input and display is used in the circuit. Carry output of the first half adder module acts as a C input for next full adder module and carry output of first full adder act as carry input for next full adder. A same procedure has been adopted for next adder modules. Sum outputs of all adder modules are connected to unsigned hexadecimal display. A and B input of all adders are supplied by one bit of hexadecimal input.

MICROWIND and DSCH 3.1 designing tool has been used for the schematic designing of this 4-Bit signed adder circuit. MICROWIND 3.1 is a VLSI designing tool in which schematic and layout designing of digital circuits can be done. DSCH is a digital schematic designing tool which deals in front end designing. In DSCH a program file known as verilog file can be generated which can be picked up by the MICROWIND back end designing tool for compilation. Performance estimation parameters such as power and area consumption can be observed at backend designing tool MICROWIND where the estimations can be done on different designing levels [11].
Proposed 4-bit signed adder has been proven best in terms of area as compared to CMOS, TG and GDI adder design. Comparative analysis of various 4-bit signed adders on 120nm has been shown in Table 1. 4-Bit signed adder design using conventional CMOS technology consists of 120 transistors, TG Up-Down counter constitutes 78 transistors and GDI and PTL Up-Down counter consists of 42 transistors.

**TABLE 1.**

<table>
<thead>
<tr>
<th>4-Bit Signed Adder</th>
<th>CMOS</th>
<th>TG</th>
<th>GDI</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>No. of NMOS</strong></td>
<td>60</td>
<td>39</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td><strong>No. of PMOS</strong></td>
<td>60</td>
<td>39</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td><strong>Width (µm)</strong></td>
<td>127.3</td>
<td>101.4</td>
<td>49.6</td>
<td>49.6</td>
</tr>
<tr>
<td><strong>Height (µm)</strong></td>
<td>14.2</td>
<td>13.2</td>
<td>12.9</td>
<td>12.7</td>
</tr>
<tr>
<td><strong>Area (µm²)</strong></td>
<td>1802.9</td>
<td>1338.5</td>
<td>639.8</td>
<td>630.4</td>
</tr>
</tbody>
</table>

Layout generation is necessary before actual implementation of any digital circuit. It is difficult to conduct the manual layout of any complex circuit which has been implemented thousands of transistors. So some time automatic layout generation approach is preferred. Transistor level design of any required circuit has been firstly designed using digital schematic editor and also logically validated at logic level.
and transistor level by observing timing simulation. A coded file known as verilog file is generated by the DSCH 3.1 designing tool. This coded file is compiled by the MICROWIND 3.1 designing tool to automatically generate the layout with exact desired design rules. This approach is used to avoid any LAMBDA rule error. The MOS generator option provided in the MICROWIND tool can be used to adjust the W and L of a transistor [11]. Generated layout consist number of metal layers and polysilicon layers. Layout of 4-bit signed adder has been shown in Fig. 7 and corresponding analog simulation has been shown in Fig. 8.

**Fig. 8. Analog Simulation of Proposed 4-bit signed adder**

**SIMULATION RESULTS**

MICROWIND 3.1 VLSI designing tool has been utilized for performing the parametric analysis of the design in terms of area and power consumed. The power consumption with respect to the applied voltage has been obtained by performing the analog simulation of the proposed adder design. Two MOSFET empirical models namely Level-3 and BSIM Model-4 have been used to get parametric analysis of proposed adder at five different supply voltages. Threshold voltage taken as 0.4V at 27°C operating temperature, MOS empirical model Level-3 and BSIM Model-4 provide with 10 and 19 different curve fitting parameters respectively. The graph for variation in power with respect to $V_{DD}$ has been shown in Fig.9 for BSIM-4 and in and Fig. 10 for LEVEL-3 MOS model. Power consumption at 1.2V on BSIM-4 MOS empirical model is 27.613µW and it is 7.877 µW on LEVEL-3 for same $V_{DD}$. As supply voltage increases power consumption also increases for both empirical models.
Fig. 9. Power vs. Supply Voltage on BSIM-4

Fig. 10. Power vs. Supply Voltage on LEVEL-3
CONCLUSION

According to present trends in the portable device industry there is a huge demand of area and power efficient electronics circuits and devices. As in portable devices there is requirement of both, less power dissipation and less area consumption, which makes us, look for those VLSI designing techniques which are both, area and power efficient. In order to meet both the constraints at the same time, an alternative 4-bit signed adder design by using PTL approach has been proposed and is implemented using 42transistors. The design implementation uses 21 NMOS and the equal number of PMOS transistors. The 4 Bit adder has been designed by incorporating three area efficient 10Transistor, PTL based full adder module and one half adder module. To analyze area and power requirements of the proposed design analytically we have used LEVEL-3 and BSIM-4 analytical models on 120 nm. The area requirement comes out to be 630.4 µm\(^2\) and the power consumed at 1.2 V comes out to be 7.877 µW using LEVEL-3 model.

REFERENCES


